VLSI Project 2 Report

1. Full schematic of your circuit (showing proper FET widths and lengths) Here the widths must match series/parallel total resistances in addition to pMOS & nMOS mobility corrections. (5pt)

a. State your transistor width choices and why.

b. Screenshot must include your username at the top of the window.

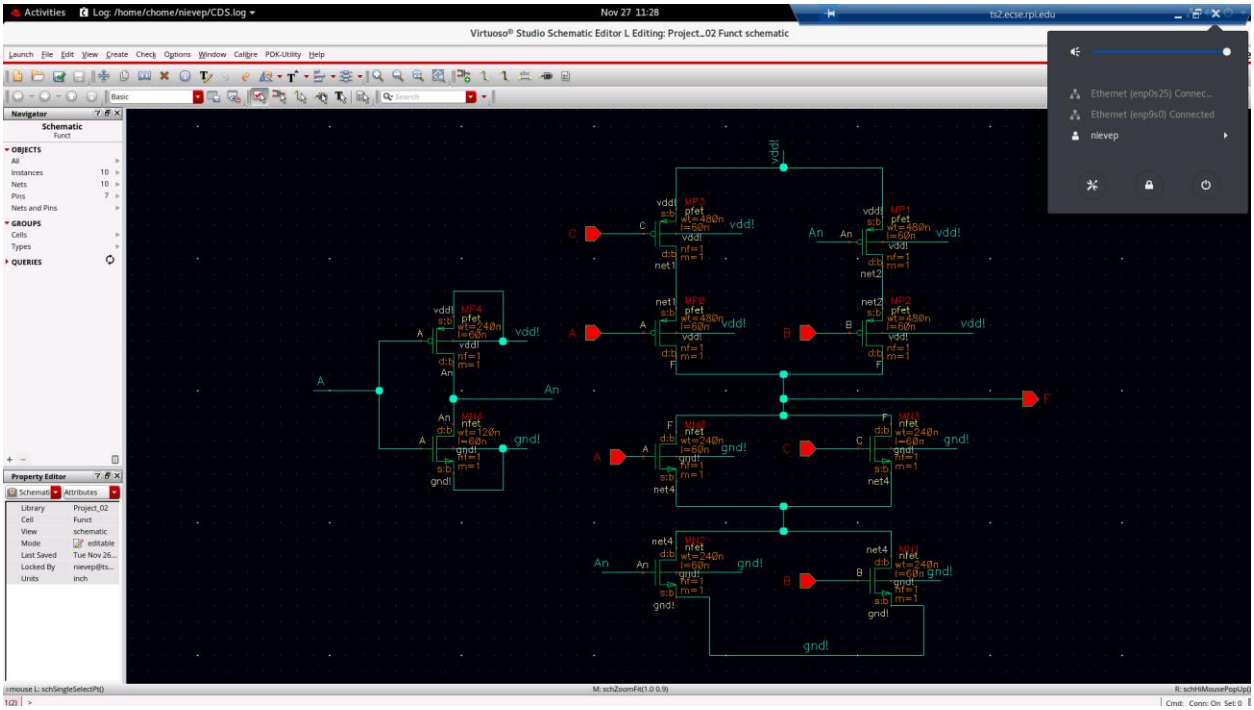

Figure X: Schematic of the Function F

2. Full layout of a compact functional cell. (15pt)

a. All transistors in layout must have a length of 60nm, same as used in the inverter.

b. Source/Drain sharing must be used whenever possible.

c. Interconnect lengths are to be minimized.

d. Justify your transistor placement in the layout.

e. State the total size of your layout (overall length x width in μm^2).

f. Screenshot must include your username at the top of the window.

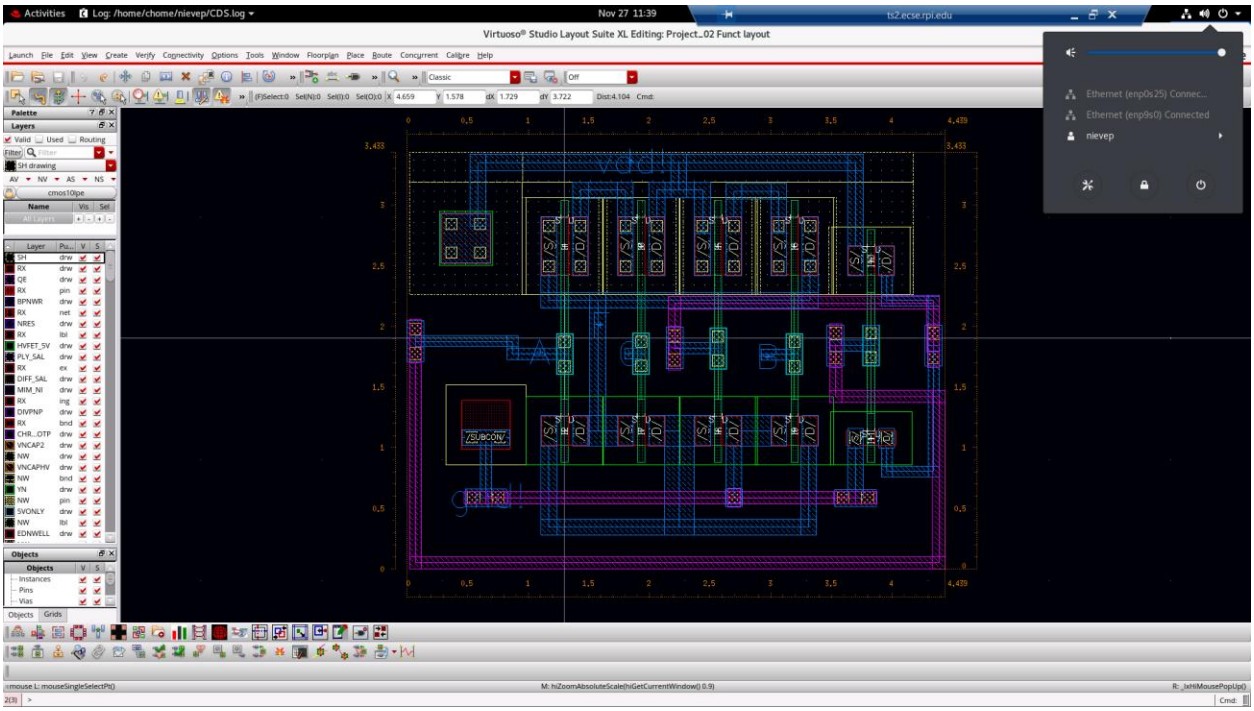

Figure X: Layout of Function F (Total size = 3.433 um x 4.439 um = 15.239 um^2)

3. Design rule check (DRC) result of the layout (show dialogue box with confirmation of clearance of DRC). (10pt)

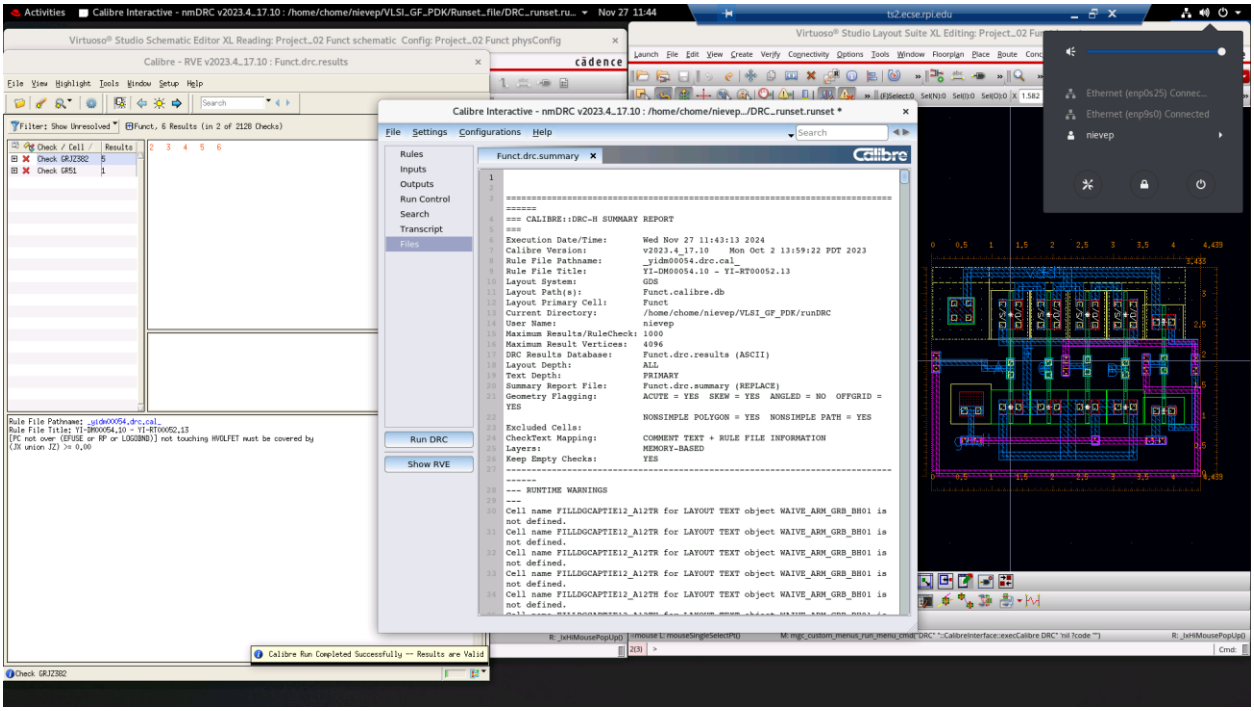

Figure X: DRC Check for Function F Layout

4. Layout extraction and Layout vs. Schematic (LVS) and parasitic extraction (PEX) check results. (10pt)

a. For LVS, screenshot the LVS si.out output log window.

b. All text from “The net-lists match.” and above must be visible.

c. Show the # of xRC warnings and 0 xRC errors from the Calibre Interactive window.

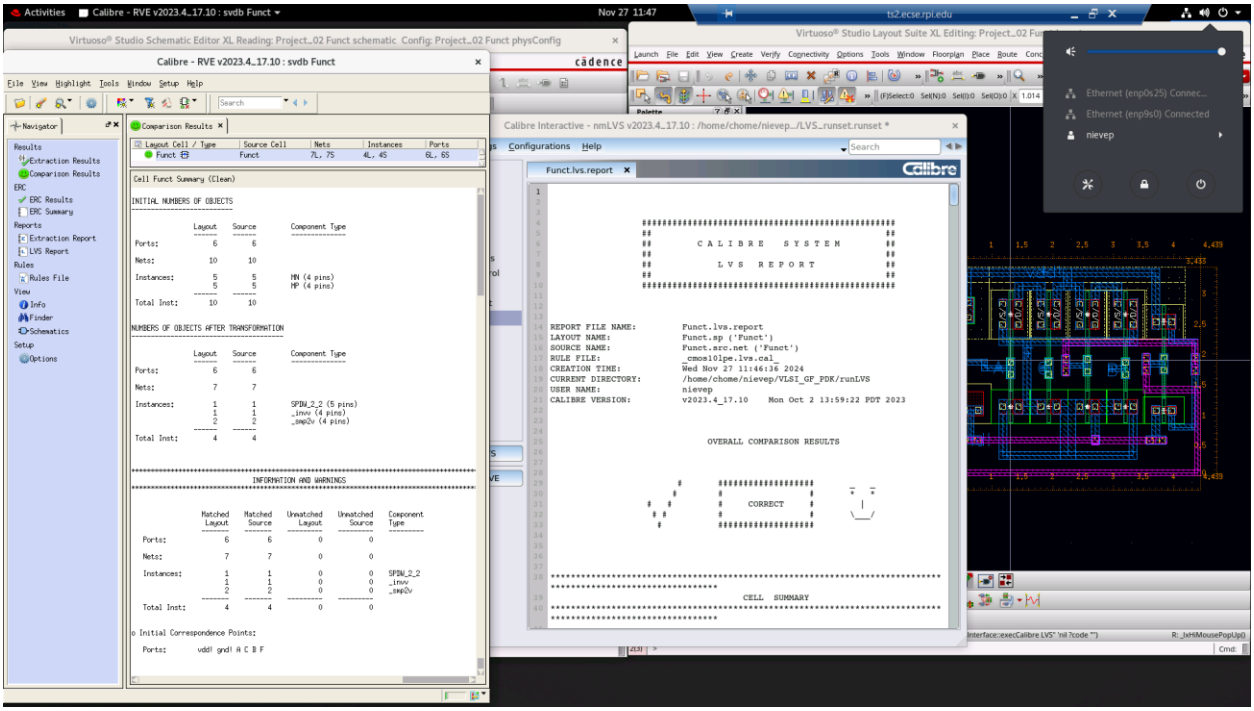

Figure X: LVS Check for Function F

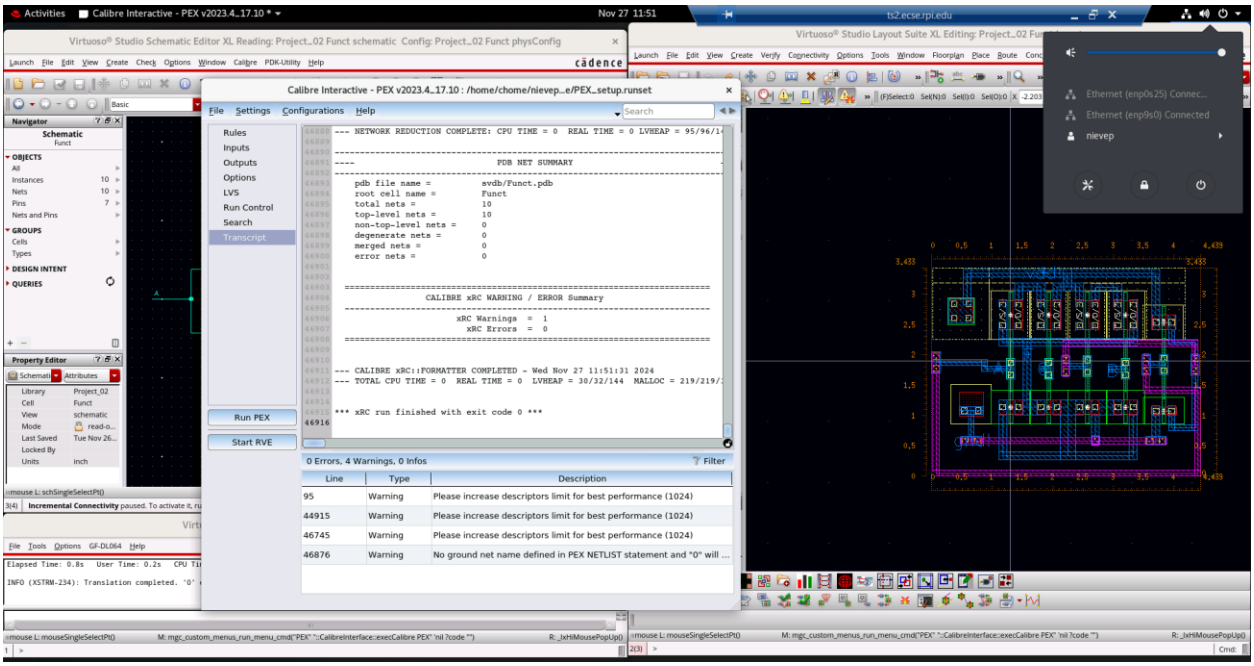

Figure X: PEX Extraction for Function F

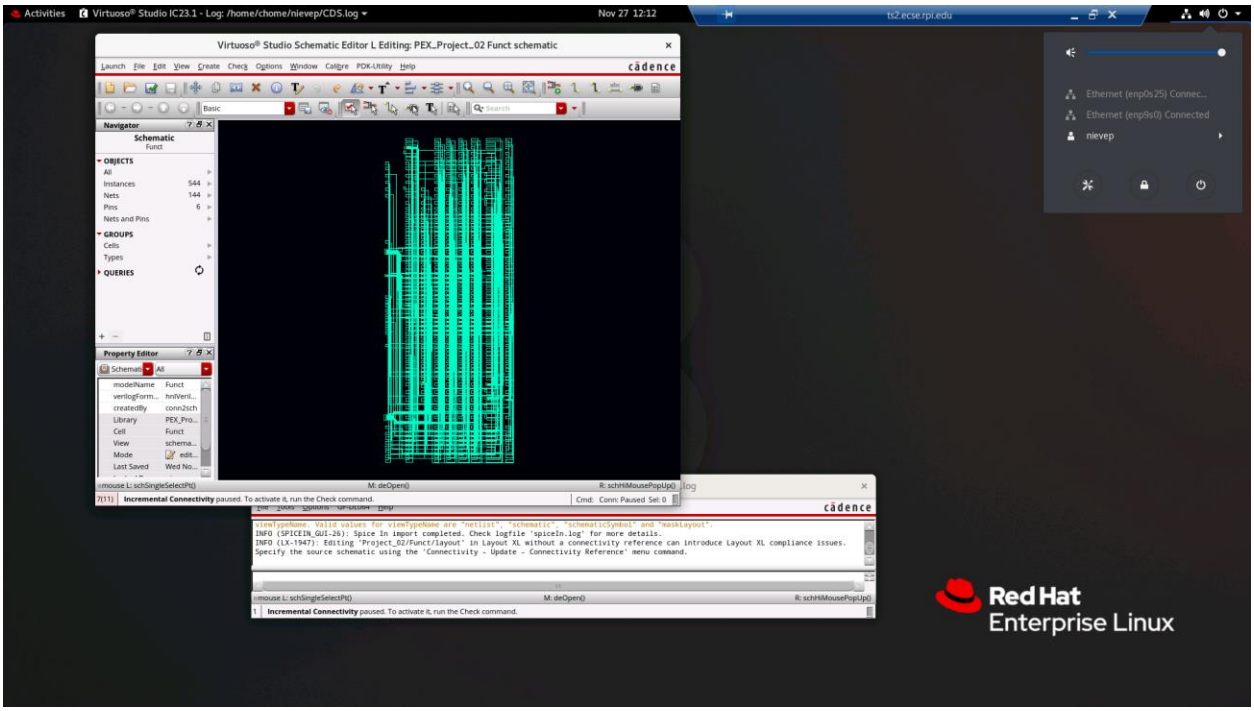

Figure X: PEX Schematic after loading Extraction

5. Find the highest frequency you are able to reliably simulate your implementation of the function with a 0.5 fF load capacitor (15pt)

a. Include both schematic and post-layout simulated result. Discuss the difference between schematic simulation result and post-layout.

b. Edit vpulse as necessary to set the fastest input pattern possible while VOH and VOL still reach 90% and 10% of VDD, respectably, with correct output.

c. You should fix the other inputs while checking the output for one input that changes.

d. State and explain any unexpected results.

e. Screenshot plots must include the time stamp from when the simulation was run (see below).

Compared to the original simulation without parasitics there is a noticeable increase in the output pulse rise and fall times (slower responses) due to the added parasitic capacitances. In the PEX extraction simulation, the rise time is measured at 11.609 ps, and the fall time is 14.0 ps. In contrast, the ideal simulation shows a faster response, with a rise time of 10.979 ps and a fall time of 9.0 ps. Additionally, the PEX extraction simulation with a 0.5 fF load and a 0.2 ns period (equivalent to a 5 GHz frequency) represents the fastest achievable frequency where the output voltages (VOH and VOL) still reach 90% and 10% of VDD, respectively, ensuring correct output functionality.

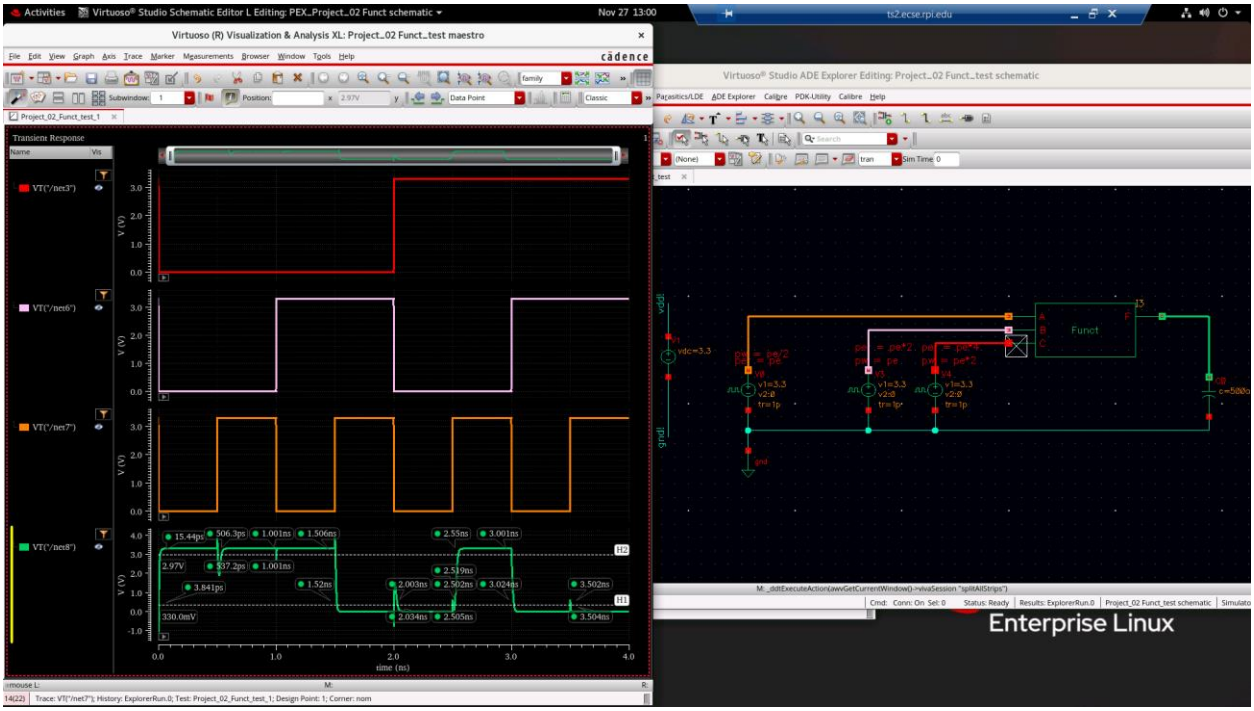

Figure X: PEX Extraction Simulation with 0.5 fF Load Results and 1 ns Period

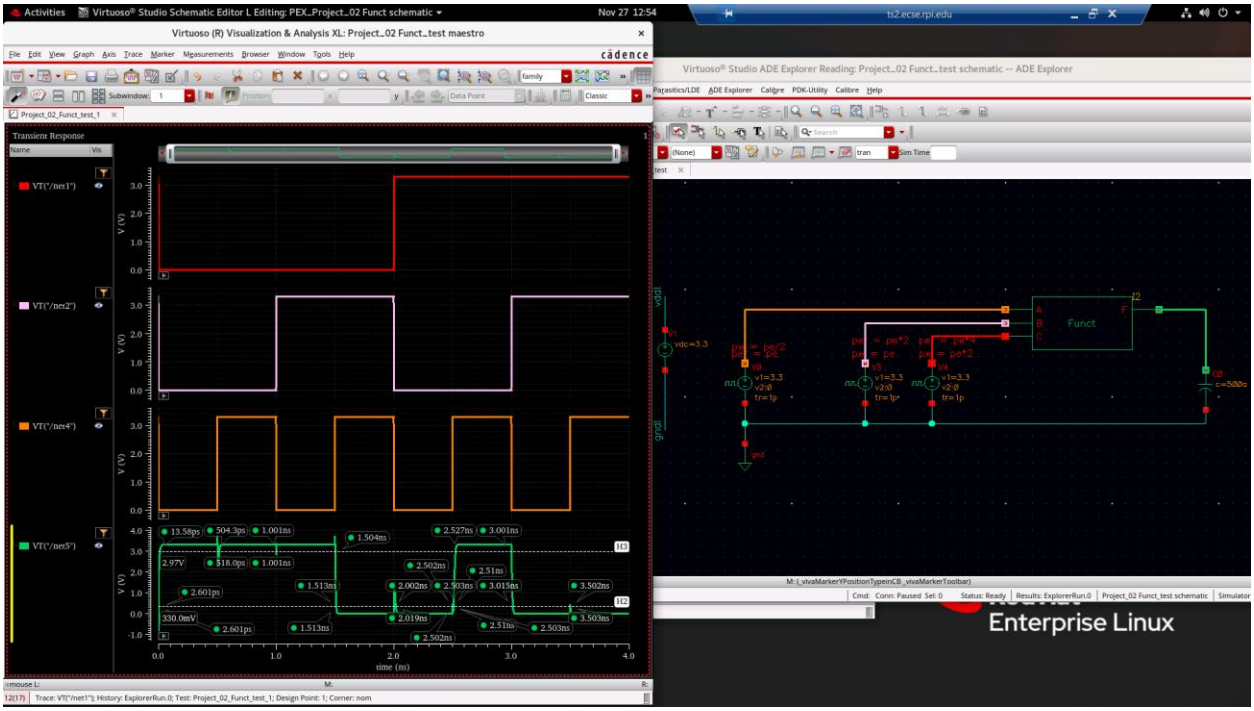

Figure X: Ideal Schematic Simulation with 0.5 fF Load Results and 1 ns Period

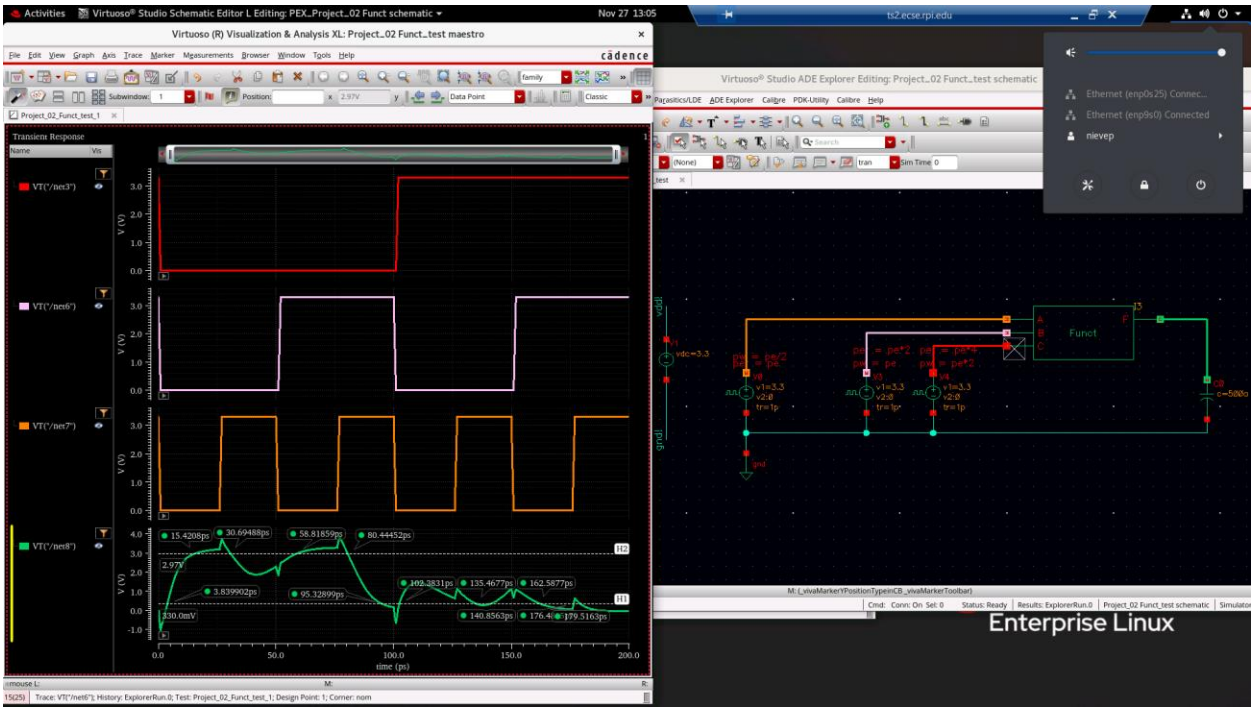

Figure X: PEX extraction Simulation with 0.5 fF Load and 0.05 ns period

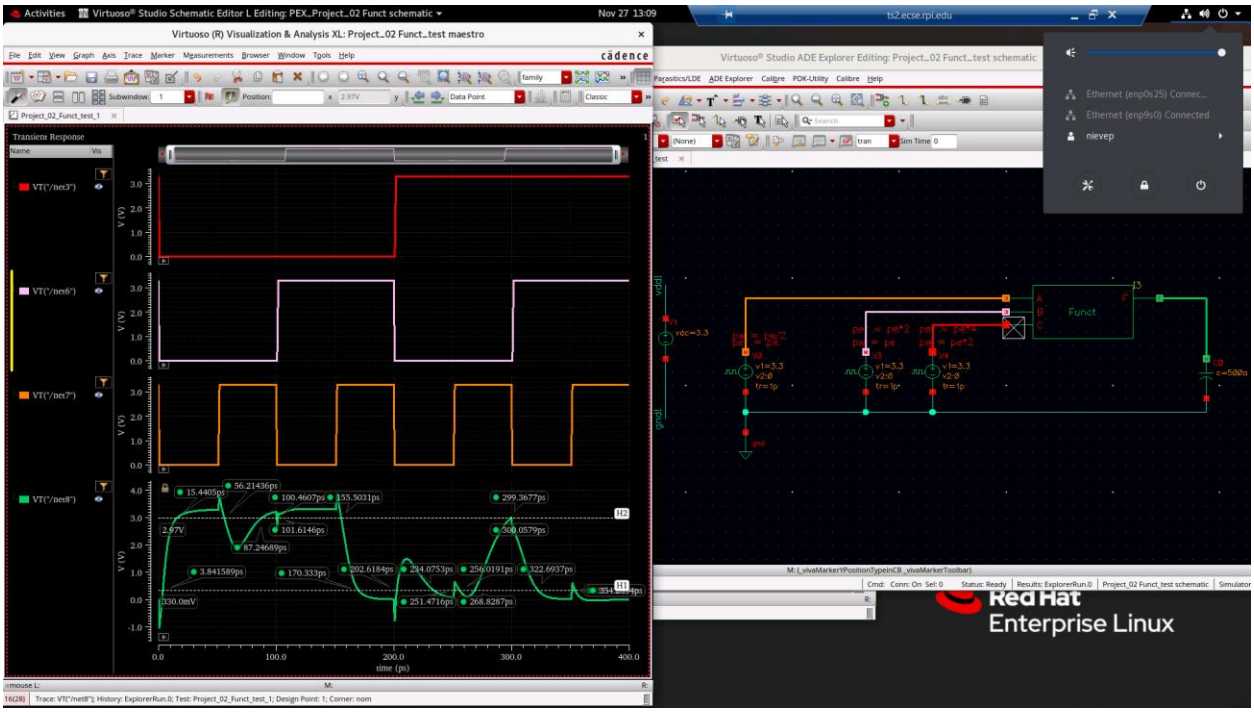

Figure X: PEX extraction Simulation with 0.5 fF Load and 0.1 ns period

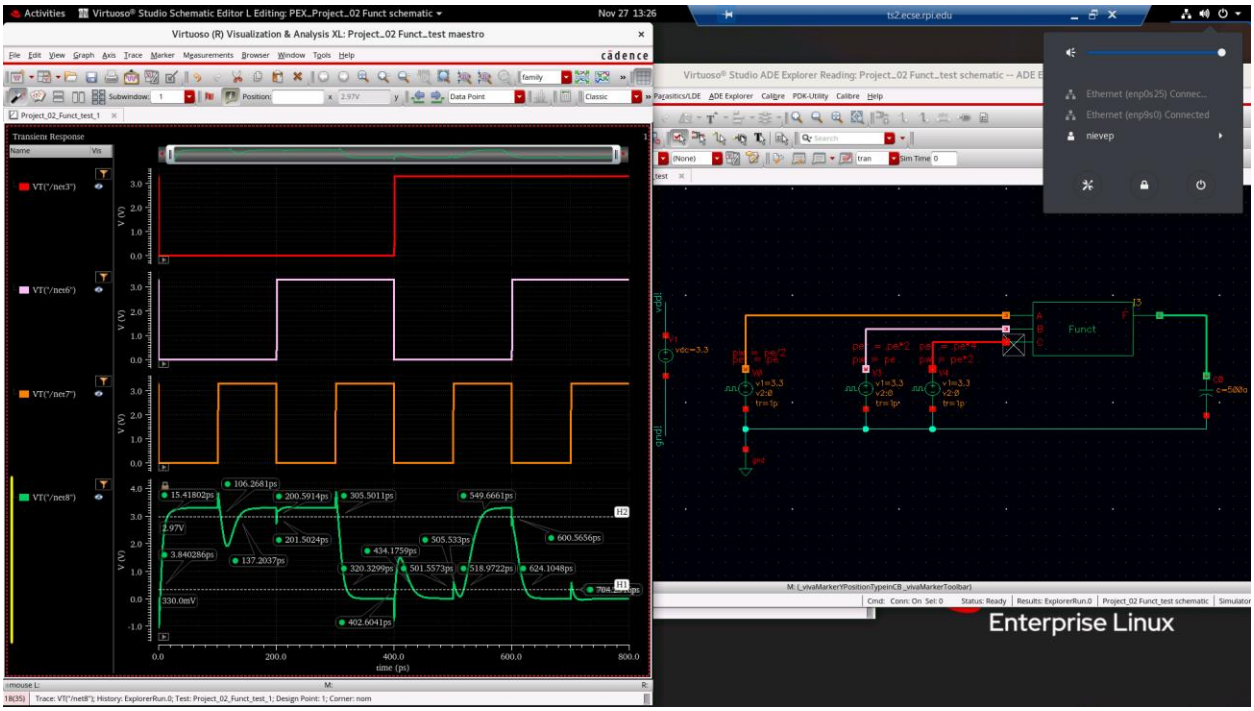

Figure X: PEX extraction Simulation with 0.5 fF Load and 0.2 ns period

6. Repeat Part 5 with a 15 fF load capacitor. (15pt)

Compared to the original simulation without parasitics, there is a noticeable increase in the output pulse rise and fall times, indicating slower response times due to the added parasitic and load capacitances. In the PEX extraction simulation with a 15 fF load, the rise time is measured at 129.45 ps and the fall time at 138.402 ps, both of which are significantly slower than the ideal case. Additionally, the PEX extraction simulation with a 15 fF load and a 0.6 ns period (equivalent to 1.6667 GHz) demonstrates that the output voltages (VOH and VOL) still reach 90% and 10% of VDD, respectively, ensuring correct output functionality.

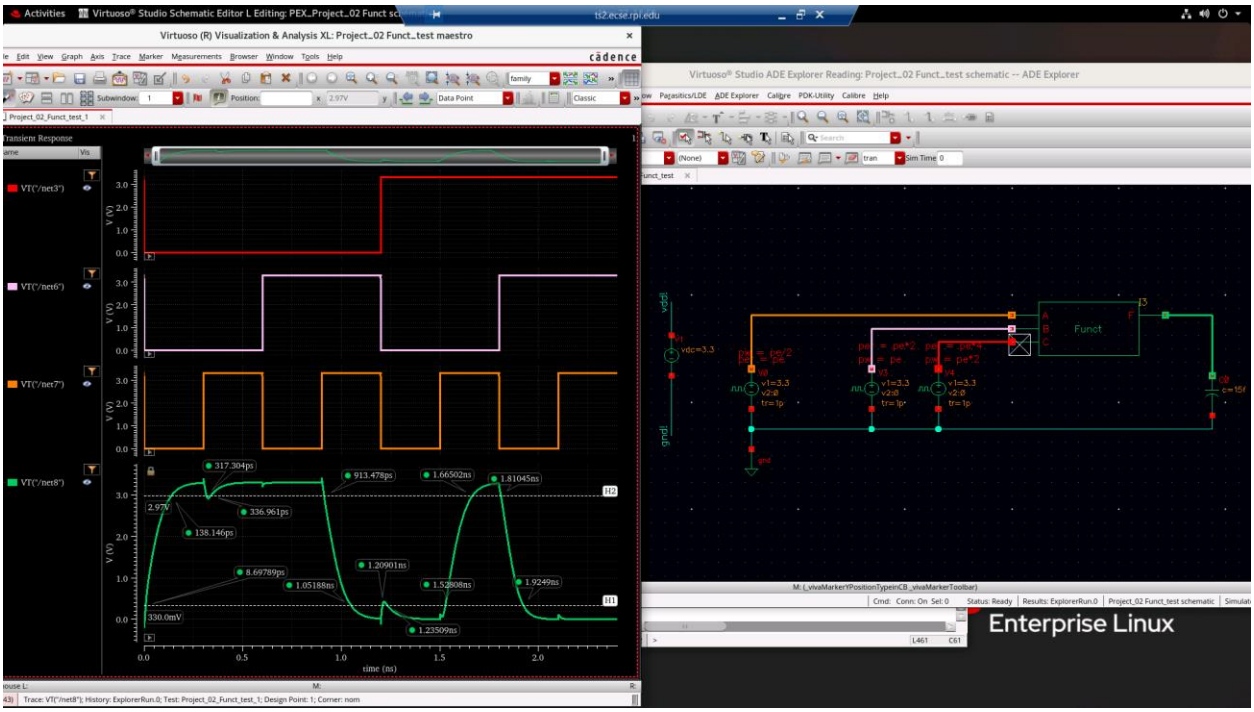

Figure X: PEX extraction Simulation with 15 fF Load and 0.6 ns period

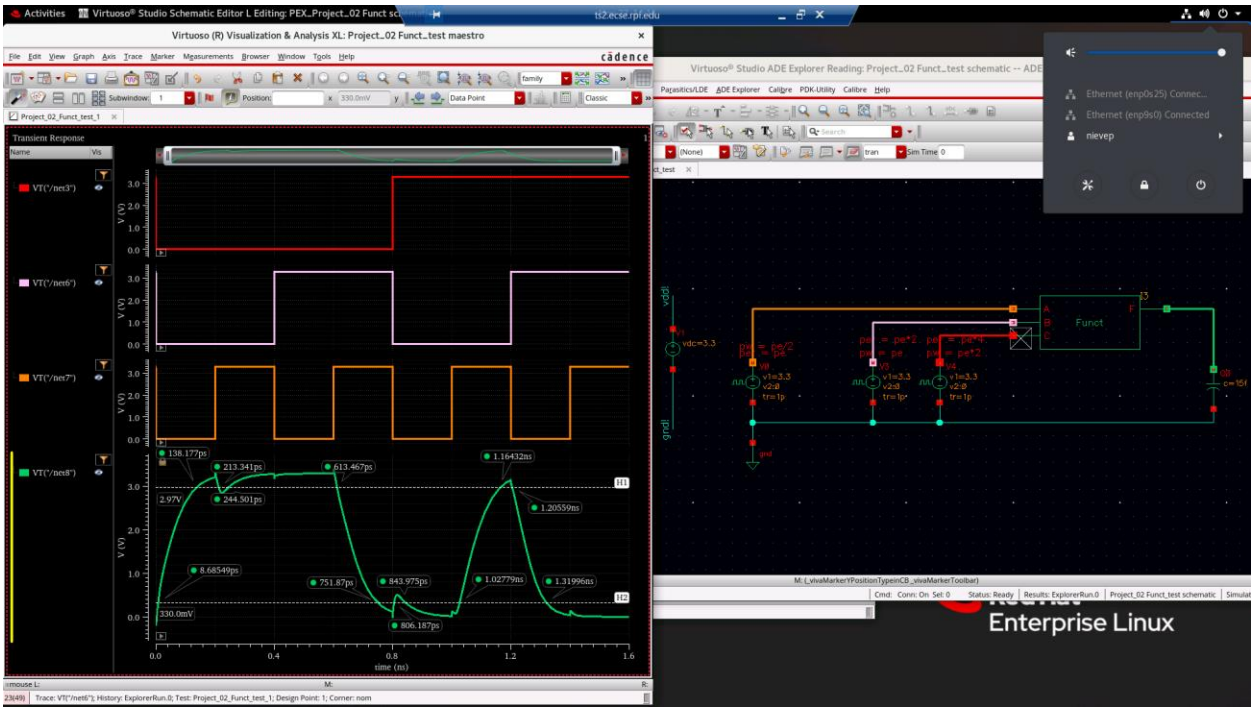

Figure X: PEX extraction Simulation with 15 fF Load and 0.4 ns period

7. Draw a concise conclusion (15pt)

a. State your final functional speed with both the 0.5 fF and 15 fF load capacitor. Explain why the differences in speed were observed. Additionally, state your propagation delay for both rising and falling output.

b. State how your design could be further improved considering the results obtained.

The final functional speeds achieved for the design were 5 GHz with a 0.5 fF load and 1.67 GHz with a 15 fF load. The speed difference arises due to the increased load capacitance, which adds parasitic effects that slow down the signal transitions. Higher capacitance causes longer charging and discharging times, increasing the rise and fall times and thus limiting the maximum frequency.

For the 0.5 fF load, the rise and fall times are faster, with minimal propagation delay, allowing for the high 5 GHz speed. In contrast, with the 15 fF load, the propagation delay increases, with a measured rise time of 129.45 ps and a fall time of 138.402 ps, leading to a lower achievable frequency of 1.67 GHz.

To further improve the design, reducing parasitic capacitances by optimizing the layout and minimizing load capacitance on critical paths could help achieve higher speeds. Additionally, adjusting the length and widths of the transistors might enhance the response time, making the design more resilient to higher load conditions while maintaining functional speed.